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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DIMYAN, MAGID Y	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 10/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/649,215	JURGENS ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This pertains to Application No. 10/649,215, filed 26 August 2003. Claims 1 – 20 are pending in this Application.

Specification

Content of Specification

2. The title of the invention is not descriptive and does not accurately reflect the claimed invention. A new title is required that is clearly indicative of the invention to which the claims are directed. An example of the suggested title is "Methodology for Generating a Modified View of a Circuit Layout".

3. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

4. The abstract of the disclosure is objected to because the abstract lacks narrative format and is merely a recitation of claim 1. Correction is required. See MPEP § 608.01(b).

Claim Objections

5. Claims 2, 3, 4, 6 and 7 are objected to because of the following informalities:

- Claims 2, 3, 4 and 7, line 2, insert --layout-- after "wafer". Claim 6, line 3, insert --layout-- after "wafer".

6. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1 – 17 and 19 - 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Dillon (U.S. Patent No. 6,093,214).

9. Regarding claim 1, Dillon discloses a method for generating a modified view of a circuit layout (see Figs. 3, 4A; col. 4, line 9 – col.4, line 16) comprising: receiving circuit layout from a design rule clean database (see col. 3, lines 44 – 53; col. 6, lines 20 – 46); extracting base wafer layout from circuit layout according to a set of instructions (see Fig. 5, block 159; col. 6, lines 20 – 34); and modifying base wafer layout according to set of instructions (see also col. 2, lines 18 – 35; col. 5, lines 11 – 16). Thus, Dillon clearly recites all the claimed limitations.

10. As per claims 2 - 5, see (7) above, as well as col. 3, line 53 - col. 4, line 34, which teach the claimed elements of the unused diffused blocks and layer tags, as well as the element of the paveover (backfill) cell.

11. Referring to claims 6 and 7, see Figs. 3 and 4A; col. 4, lines 8 – 65, which show the comparison between base layers, and the routing placements over the base layers, as claimed.

12. As for claims 8, 9 and 10, see above, as well as col. 3, lines 44 – 53, which disclose how the control layers have to conform to any design rules for a standard cell library, as claimed.

13. Pursuant to claim 11, see (7) – (8) above, as col. 7, lines 14 – 23 which teach the claimed limitation of having a database with diffused blocks that are unused in the design.

14. With regards to claims 12 and 13, Dillon discloses a design tool for automating a process for generating a modified view of a circuit layout (see (7) above, as well as col. 1, lines 12 – 32) comprising: means for extracting base layers of one or more diffused blocks of circuit layout (see Fig. 5, block 159; col. 6, lines 20 – 34); and means for forming a paveover cell comprising the extracted base layers, wherein the design tool facilitates reuse or routing resources of the diffused blocks (see (7) and (8) above, as well as col. 6, line 58 – col. 7, line 64). Thus, Dillon teaches all the claimed elements.

15. As per claim 14, see col. 1, lines 12 – 32, which teach how any commercially available tool suite can be used in the design process (HDL is well known in the art and is universally used in all commercially available tools needed for IC development and design).

16. Pursuant to claims 15 and 16, see above, as well as col. 5, line 36 – col. 6, line 2, which show the automatic (computer program with instructions stored in memory) for creating route guides, as claimed.

17. As for claim 17, see above; Fig. 5; col. 2, line 44 – col. 4, line 8, which cite the element pertaining to generating a netlist with the backfill information.

18. Referring to claims 19 and 20, see also Figs. 1, 2, 3 and 4A; col. 4, line 8 – col. 5, line 17, which clearly disclose the views of the paveover cells; and correctly comparing the base layers of the paveover cells with circuit layout base layers, as claimed.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 18 is rejected under 35 U.S.C. 103(a) as being obvious over Dillon in view of Pub. No. US 2004/0049754 A1 to Liao et al.

21. The teachings of Dillon pertaining to a design tool for automating a process for generating a modified view of a circuit layout as recited above in claim 13 are described in more detail in his disclosure. Dillon teaches (Fig. 5, block 160; col. 7, lines 3 – 13) the manual or automatic merge process identifying the closest base cell locations to an optimum placement position of the backfill cell instance and the routing of the interconnections between the standard cells and the backfill cell instances, as necessary. Dillon also teaches (col. 7, lines 38 – 52) the importance of "speeding the

time to market" for the IC. This requires good device reliability and wafer yields. But Dillon is silent on the claimed limitation cited in claim 18 of generating a metal utilization (mu) annotation file in response to a DRC operation during the routing process. On the other hand, Liao et al. provide a method and apparatus for achieving a near uniform wafer surface topography or planarization in an IC layout (paragraph 0002), and further stress the importance of monitoring the metal utilization (mu) density factor in the IC layout using DRC constraints (paragraphs 0041 and 0045) in order to improve reliability and manufacturing yields (paragraphs 0003 and 0014). Since, as stated by Liao et al. (paragraph 0014), achieving a ***desired metal utilization (mu) density in an IC layout facilitates the achievement of a global planarization***, resulting in an ***improved wafer yield and an improved reliability factor*** for the manufactured IC, it would therefore be obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Dillon and Liao et al. to obtain the same claimed invention

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

myd
26 October 2005

A. M. Thompson
Primary Examiner
Technology Center Z800